AND8207/D

19 V/6.4 A Universal Input AC-DC Adaptor with PFC Using NCP1603

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APPLICATION NOTE

INTRODUCTION

This application note presents an AC−DC converter example circuit in Figure 1 using NCP1603 with the design steps and measurement. The measurement shows that the 120 W converter has a greater than 0.93 power factor under the universal input (90 to 260 Vac), less than 200 mW no load standby power consumption, and greater than 81% efficiency. NCP1603 is a co−package of NCP1230 and NCP1601 so that the example circuit can be a reference circuit for NCP1230 and NCP1601.

The NCP1603 is first ON Semiconductor PFC/PWM (or so called PFC/DCDC because the second stage is only a DC−DC conversion) combo controller featuring integrated high−voltage startup and excellent low standby no load power consumption. The NCP1603 solution is the standard two−stage PFC−PWM power conversion. Suiting for low−power AC−DC application, the PFC section is Discontinuous Conduction Mode (DCM) and Critical Mode (CRM) boost topology. This PFC operating mode is a special case of Peak−Current Mode PFC that needs fewer external components since the average−current circuit is saved. It is suitable for space−saving in the combo controller implementation. On the other hand, the PWM section is a fixed−frequency PWM current−mode CCM or DCM flyback topology with skipping cycle capability. The features (including skipping cycle operation, the integrated lossless high−voltage startup and the PFC section shutdown during standby) present excellent no−load standby power consumption. NCP1603 is an ideal controller for application that needs extremely low standby power consumption and PFC feature.

Table 1. Features of Power Supply Using NCP1603 or NCP1230/NCP1601

	PFC Stage	PWM Stage	Features
Topology	CRM / DCM boost	CCM / DCM flyback	● CRM/DCM PFC is preferable for low−power application. CRM is a special case of Peak Current Mode PFC that needs very few external components. ● Hold−up time is maximized by a step−up voltage in the PFC. ● Isolated flyback topology is with minimum circuit component for low−power application.
Standby condition	Power off	Skipping cycle	● It offers excellent low standby power consumption.
Fault condition	Power off	Double hiccup restart	● It minimizes power dissipation in fault and allows auto−recovery ability when fault is cleared.
Latch protection activated	Power off	Latched off	● V_{CC} stays above typical 5.6 V and PWM drive output remains off until circuit reset. ● Reset needs the AC input unplugged.

The maximum input power the NCP1603 is experimentally found at around 120 W for universal input range. The major barrier for higher power is that the Go−To−Standby (GTS) feature requires higher overcurrent (OCP) level in PFC (because the PFC needed to startup at low−line full−load condition that the circuit is drawing high non−fully−power−factor−corrected current in this moment) and the OCP level is indirectly related to the zero current threshold (ZCD) of the PFC stage. Higher ZCD level will reduce the efficiency by non−zero−current switching and also make the PFC distortion higher in the high−line condition.

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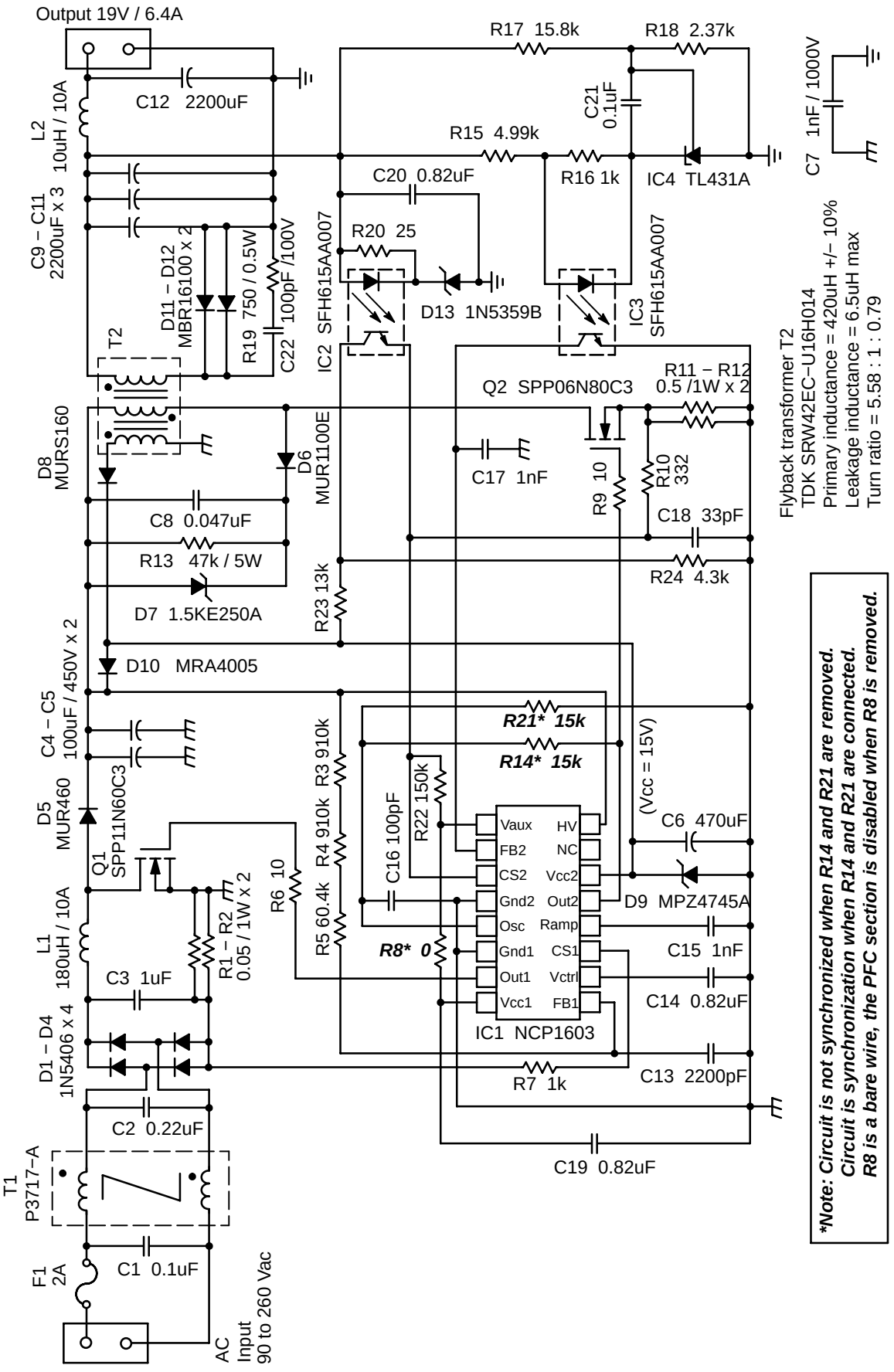

Figure 1. Application Schematic of the Example Circuit

DESIGN STEPS

Step 1. Define the Specification

Input	90 to 260 Vac, 50 Hz
Output	19 Vdc, 6.4 A, isolated
Features	Synchronization option Output overvoltage protection latch

The maximum overvoltage protection threshold of the PFC section is 225 μA that corresponds to 225 μA x 1.88 MΩ + 5 V = 428 V when feedback resistor R_{FB} is 1.88 MΩ (910 kΩ + 910 kΩ + 60 kΩ) and a 5 V maximum offset of the feedback pin of the PFC section. A 450 V output capacitor can be used here. On the other hand, the output voltage has to be higher than the maximum of input voltage in boost topology to make the boost converter work properly. Therefore, the nominal PFC−stage output voltage V_{out} is set at 380 Vdc. Note that there is a roughly 4 V offset when feedback current is 200 μA.

$$V_{out} > V_{in(max)} = \sqrt{2} \cdot 260 = 367.7\ V$$

$$V_{out} = 200\ \mu A \times 1.88\ M\Omega + 4\ V = 380\ V$$

In order to demonstrate the PFC/PWM synchronization option, the DCM frequency of the PFC is chosen to be around 100 kHz so that it matches the PWM section operating frequency in the synchronization case. Referring to Figure 70 in the NCP1603 datasheet when a 100 pF capacitor is connected to osc pin (Pin 5), the PFC section maximum frequency is clamped at 107 kHz that corresponds the DCM operation switching period as 9.33 μs.

$$f = 107\ kHz$$

$$T = \frac{1}{f} = 9.33\ \mu s$$

Step 2. Assuming Efficiency and Loss

The converter consists of two power stages. The overall efficiency is a cascaded efficiency of the two stages. Hence, the target overall efficiency cannot be too aggressive. When both stages are with 90% efficiency, the overall efficiency η is only 81%. It means that 150.1 W input power P_{in} is needed to deliver 19 V/6.4 A at 81% efficiency. Referring to Figure 2, only 135 W power is needed from the PFC stage but the PFC stage is designed at 150 W to reserve some design margin.

$$P_{in} = \frac{P_{out}}{\eta} = \frac{19\ V \times 6.4\ A}{81\%} = 150.1\ W$$

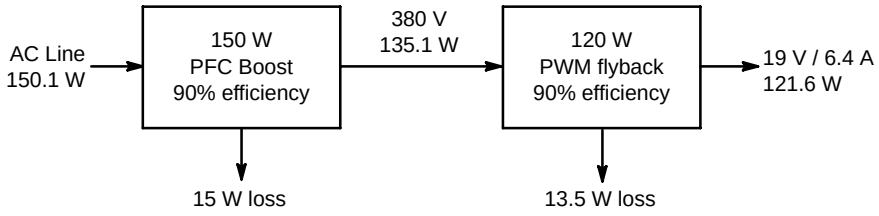

Figure 2. Power Structure

Step 3. Biasing the Controller

Thanks to the high−voltage startup pin (Pin 16) of the NCP1603, the initial IC supply voltage V_{CC} can be obtained by connecting this pin to the bulk capacitor voltage in Figure 3. In order to have extremely low standby power consumption, the V_{CC} must be supplied by an external biasing circuit that costs only one additional output of the flyback in the PWM stage.

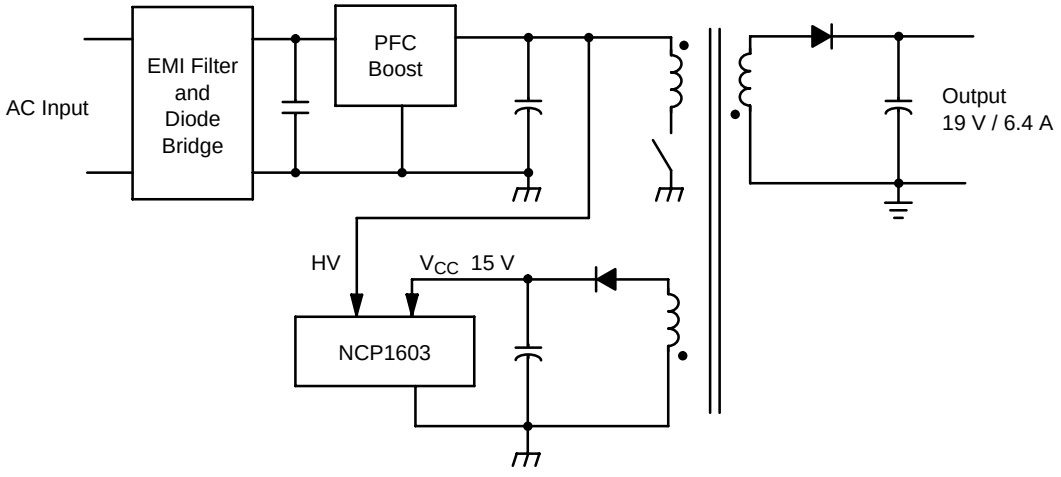

Figure 3. V_{CC} Biasing Scheme

Typical total current consumption of the whole NCP1603 controller (including the PWM and PFC sections and the current to switch a pair of MOSFETs) are 10 mA. The supply voltage is normally set as 15 V so that it reserves some margin for the startup threshold of the PFC section (typical 10.5 V) to avoid insufficient biasing voltage.

Step 4. PFC Section Design

The PFC Section of NCP1603 is NCP1601. So, the design is a standard PFC NCP1601 circuit design as follows.

Step 4a. Calculate the Current Stress

The worst case happens when input is 90 Vac. The input RMS current I_{ac} is 2.22 Aac if the power factor is perfect. The suffix ac represents it is RMS value. This current stress is mainly on the front−ended rectifier.

$$P_{in} = \frac{P_{out}}{\eta} = \frac{150}{90\%} = 167\ W$$

$$I_{ac} = \frac{P_{in}}{V_{ac}} = \frac{167\ W}{90\ V} = 1.85\ Aac$$

The instantaneous maximum current stress in the PFC stage will be 6.29 A in critical mode.

$$I_{pk} = 2\sqrt{2}\, I_{ac} = 5.24\ A$$

This current stress affects the component selections on the current sense resistor, MOSFET, diode and inductor.

Step 4b. Inductor Design

The minimum CRM inductance $L_{(CRM)}$ at low line is obtained as follows:

$$L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{I_{pk}} \frac{1}{f}$$

$$= \frac{380 - \sqrt{2} \cdot 90}{380} \frac{\sqrt{2} \cdot 90}{6.29} \frac{1}{107 \times 10^3} = 151\ \mu H$$

It is the minimum value inductor value to keep the circuit in CRM. The inductor L is therefore set to be 180 μH. The switching frequency is 75 kHz at the sinusoidal peak and it is in CRM.

$$L = 180\ \mu H$$

$$freq = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{I_{pk}} \frac{1}{L}$$

$$= \frac{380 - \sqrt{2} \cdot 90}{380} \frac{\sqrt{2} \cdot 90}{5.24} \frac{1}{180 \times 10^{-6}}$$

$$= 88\ kHz < 107\ kHz$$

Step 4c. Ramp Capacitor Design

Maximum power can be obtained when $V_{control}$ = 1 V. Worst case is at low line 90 Vac.

$$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2LI_{ch}$$

$$= \frac{167}{90^2} \cdot 2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} = 742\ pF$$

Hence, the C_{ramp} is set to be 1 nF.

$$C_{ramp} = 1000\ pF$$

With this value of C_{ramp}, the $V_{control}$ in high line and low line conditions are 0.11 V and 0.89 V respectively.

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 167}{10^{-9} \cdot 260^2} = 0.09\ V$$

$$V_{control} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$$

$$= \frac{2 \cdot 180 \times 10^{-6} \cdot 100 \times 10^{-6} \cdot 167}{10^{-9} \cdot 90^2} = 0.74\ V$$

Step 4d. Adjust the Output Voltage

When $V_{control}$ is estimated, the output voltage can be estimated more accurately by the 96% regulation block. The calculation here takes a 4 V offset at around the feedback current range of I_{FB} = 200 μA. The output voltage in the high line and low line conditions are 378.67 V and 368.86 V.

$$V_{out} = (V_{out(nom)} - 4\ V) \cdot (1 - 0.04 \cdot V_{control}) + 4\ V$$

$$= (380 - 4)(1 - 0.04 \cdot 0.09) + 4 = 378.67\ V$$

$$V_{out} = (V_{out(nom)} - 4\ V) \cdot (1 - 0.04 \cdot V_{control}) + 4\ V$$

$$= (380 - 4)(1 - 0.04 \cdot 0.74) + 4 = 368.86\ V$$

Step 4e. Check the Switching Period to Ensure CRM at the Sinusoidal Peak.

The switching period in high line and low line conditions are:

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{378.67}{378.67 - \sqrt{2} \cdot 260} \frac{10^{-9} \cdot 0.09}{100 \times 10^{-6}}$$

$$= 30.64\ \mu s > 9.33\ \mu s$$

$$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}} \frac{C_{ramp}V_{control}}{I_{ch}}$$

$$= \frac{368.86}{368.86 - \sqrt{2} \cdot 90} \frac{10^{-9} \cdot 0.74}{100 \times 10^{-6}}$$

$$= 11.31\ \mu s > 9.33\ \mu s$$

When the circuit operates in CRM at the peak, the maximum current is limited to twice of the average.

Step 4f. Current Sense Resistors Design

There is a minimum sense resistor limit of $R_{S(ZCD)}$ = 1 kΩ. The higher the R_S value, the higher the current sense resistor needed which dissipates more power. Therefore, R_S is set at 1 kΩ.

$$R_S = 1\ k\Omega$$

Then, the maximum inductor current from the previous step is 5.24 A in low line is with R_{CS} = 37.6 mΩ.

$$R_{CS} = \frac{R_S \cdot I_{S(OCP)} - V_{S(OCP)}}{I_{L(OCP)}}$$

$$= \frac{1\ k\Omega \cdot 200\ \mu A - 3.2\ mV}{5.24\ A} = 31.3\ m\Omega$$

Then, R_{CS} is set at parallel of two 50 mΩ resistors to make $I_{L(OCP)} > 6.29$ A. It gives the maximum current limit $I_{L(OCP)}$ is 5.24 A.

$$R_{CS} = 25\ m\Omega$$

$$I_{L(OCP)} = \frac{R_S \cdot I_{S(OCP)}}{R_{CS}}$$

$$= \frac{1\ k\Omega \cdot 200\ \mu A - 3.2\ mV}{25\ m\Omega} = 7.87\ A$$

Step 4g. Bulk Capacitor Design

As a rule of thumb, output capacitance is generally set at 1 μF/W. Hence, without loss of generality the 150 W application needs 150 μF. Another consideration is the ripple current in the bulk capacitor.

On the other hand, in a NCP1601 PFC circuit the instantaneous output voltage affects the instantaneous control voltage $V_{control}$. If the output voltage ripple is too high, it will make a large ripple on control voltage and the power factor can be dramatically reduced for highly dynamic control voltage.

Hence, it is implemented by two 100 μF, 450 V capacitors to increase the ripple current capability.

$$C_{bulk} = 200\ \mu F$$

Step 4h. Fine Tuning Capacitor on $V_{control}$ Pin

The unity power factor in the NCP1601/NCP1603 PFC circuit greatly relies on how steady the control voltage in the $V_{control}$ pin (Pin 10). A large external capacitor on this pin can help to reduce the noise and dynamics of this voltage and give a decent power factor. However, if the capacitor is too large, it will reduce the dynamic response or startup transient of the circuit.

Step 5. PWM Section Design

The PFC Section of NCP1603 is NCP1230 flyback that is fixed−frequency PWM and generic approach can be used.

Step 5a. Fixed−Frequency PWM Flyback Calculation

In order to have extremely low standby power consumption, the PWM flyback always operates. The flyback is needed to be capable of the cases when the PFC boost is operating or not. Hence, the input voltage of the PWM flyback circuit must be wide input range. Some design margin is taken here. The high and low line voltages are assumed to be 100 V and 420 V respectively.

$$V_{in(L)} = 100\ V$$

$$V_{in(H)} = 420\ V$$

Because the transformer turn ratio is variable in the design of a flyback circuit, the design is an iteration process to balance a set of parameters to make the parameters work nicely with each other. The following are the most concerned parameters.

- **Maximum duty ratio** − It is a parameter limited by the switching controller and cannot go further if the switching controller is not replaced. It is (75% min, 85% max) for NCP1230 (the PWM section of the NCP1603). This is the first constraint.
- **Minimum duty ratio** − The NCP1230 enters skipping mode when V_{FB2} goes below 0.75 V (typical). It corresponds to duty goes below 20% (typical) (V_{FB2} = 3 V for 80%). The flyback has minimum duty ratio when the PFC is on and the circuit is delivering full power. It is undesirable to have skipping operation in full load due to potential low−frequency audible noise.
- **Maximum MOSFET voltage stress** − It includes the reflected voltage and the possible instantaneous peak voltage due to the leakage inductance of the transformer. Common available MOSFET voltage in market is up to 800 V. This is another constraint.
- **Maximum output diode blocking voltage** − The blocking voltage increases with the forward voltage drop. This conduction loss is significant because the output current in this design is 6.4 A.
- **Maximum input power for a realistic efficiency (or output power)** − It is done by selecting the maximum peak current, inductance (to affect the operating mode in CCM or DCM).

To keep this application note short enough and readable, the iteration process is not shown.

According to the calculation result, the following parameters are finalized:

Output voltage = 19 V

Output current = 6.4 A

Output diode volt drop = 1 V

Transformer turn ratio (n1/n2) = 5.58

Maximum peak switch current = 4 A

Switching frequency = 100 kHz

Transformer primary inductance = 420 μH

Duty ratio (at V_{in} = 420 V, Continuous mode lossless) = 21%

Duty ratio (at V_{in} = 100 V, Continuous mode lossless) = 53%

It is noted that the minimum duty ratio in this design is a little bit low. Customers are recommended to design it higher to keep skip condition (duty < 20%) away from the normal operation.

Particularly for the NCP1230 (NCP1603 PWM section) if the maximum current limit is set at 4 A, it refers a pair of resistors R11−R12 (or R_{CS}) = 0.25 Ω.

$$I_{D(max)} = \frac{1\ V}{R_{CS}} = \frac{1\ V}{0.25\ \Omega} = 4\ A$$

The compensation ramp (that relates to stability and maximum duty) is set by R10 (or R_S). Smaller value of R_S makes a fewer compensation ramp for the modulation (less stable) and allows more maximum duty. Typical starting point of R_S for design is from 1 kΩ or 2 kΩ. When stability problem is encountered, the value of R_S is needed to be increased or the voltage−loop feedback gain is needed to be reduced.

Step 6. V_{CC} Capacitor

The maximum allowable time to recognize a fault is 125 ms and the V_{CC} voltage is supposed to be still higher than the minimum operating values and hence the capacitor should be larger than 56 μF.

$$C = \frac{Idt}{dV} > \frac{2.2\ mA \cdot 125\ ms}{12.6\ V - 7.7\ V} = 56\ \mu F$$

Another concern on V_{CC} capacitor selection is to make sure that V_{CC} voltage is always above the UVLO start threshold (10.5 V typical) of the PFC section in standby where the ripple is higher.

Step 7. Decoupling Capacitors

Noise is always generated in the switching mode power supply. Some cautions are taken to handle the noise on some pins regarding the NCP1603 as following. The values of the decoupling capacitors are all up to the noise level in the layout.

FB1 pin (Pin 9): Noise on this pin will potentially trigger the PFC OVP and the PFC operation can be ruined completely.

CS2 pin (Pin 3): Noise on this pin will trigger the latch protection that is needed to be reset by unplugging the main (or making V_{CC} goes below 4 V).

FB2 pin (Pin 2): Noise on this pin will affect the PWM section duty ratio generation.

Vaux or V_{CC1} pins (Pin 1 or 8): The internal Vaux MOSFET is with 11.7 Ω typical resistance. It is high enough to pollute the V_{CC1} voltage through the high−frequency switching pulses or noise. A decoupled capacitor is needed to keep V_{CC1} voltage clean.

Step 8. PFC on/off Toggling

The NCP1603 circuit turns the PFC section on and off depending on the load conditions by the changing of PWM section feedback voltage V_{FB2}. There may be a potential on/off toggling issue when the load condition is at the on/off boundary. A resistor R22 is recommended to be connected between Vaux pin (Pin 1) and CS2 pin (Pin 3) to solve the toggling issue. This resistor adds an offset voltage to CS2 pin when Vaux is high and it reduces the variation of V_{FB2} between the PFC−on and PFC−off.

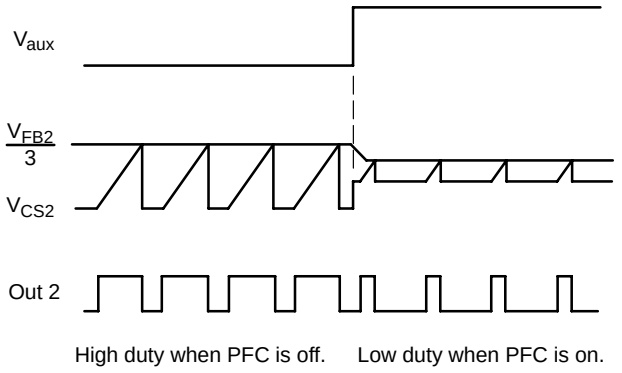

Figure 4. Transition when PFC turns on.

Step 9. PCB Layout

Layout is a big issue for the PFC/PWM combo controller because the shortest distances between the NCP1603 controller and the PFC MOSFET, PWM MOSFET and opto coupler are wanted. It is also noticed that the controller should be located outside the high current loop to prevent the strong magnetic field interfere the controller operation. The layout stretch of the example circuit is shown in Figure 5.

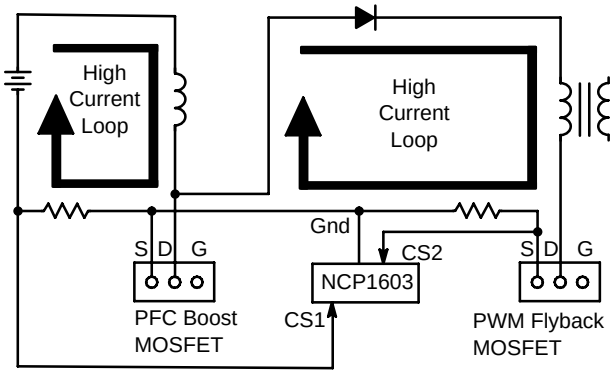

Figure 5. Layout Stretch

MEASUREMENT

Part I. Standby loss

The circuit offers excellent no load standby performance. The power consumption of the 150 W circuit is less than 200 mW. When input is high line (260 Vac) and the output is 508 mW (19.07 V * 26.66 mA), the input power is 840 mW.

Input	Input power
260 Vac	180 mW
230 Vac	150 mW
220 Vac	145 mW
200 Vac	130 mW
160 Vac	110 mW

Part II. Operating and Not Synchronized

The PFC section of NCP1603 is in DCM sometimes. DCM operation can be synchronized with the PWM section or independently operates. This part shows the operating performance when the circuit is not synchronized. When R14 and R21 are removed, the circuit is not synchronized. In Figures 6 to 9, the upper trace is the input current with 2 A/div. The center trace is the PFC output voltage with 100 V/div. And the lower trace is the rectified input voltage with 100 V/div.

Input	Output	Efficiency	PF / THD
90 Vac 145.4 W	18.91 V 6.4 A	83.2%	0.998 / 5.2%
110 Vac 143.7 W	18.91 V 6.4 A	84.2%	0.997 / 5.2%
120 Vac 143.2 W	18.91 V 6.4 A	84.5%	0.996 / 6.3%
180 Vac 139.5 W	18.91 V 6.4 A	86.8%	0.993 / 6.3%
220 Vac 137.6 W	18.91 V 6.4 A	88.0%	0.982 / 13.3%
230 Vac 137.1 W	18.91 V 6.4 A	88.3%	0.973 / 17.9%
260 Vac 135.9 W	18.91 V 6.4 A	89.1%	0.934 / 34.2%

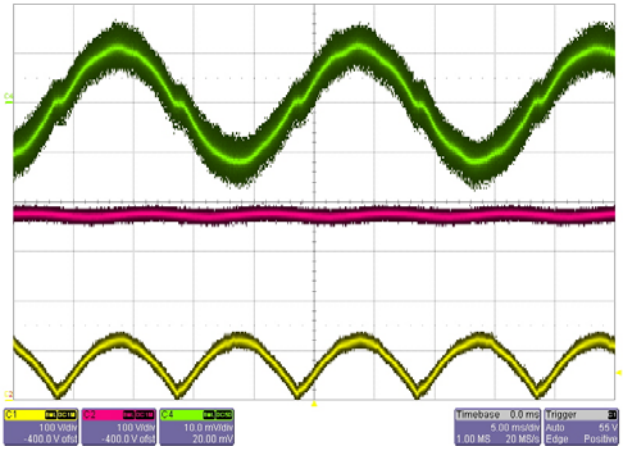

Figure 6. 90 Vac Input Voltage and Not Synchronized

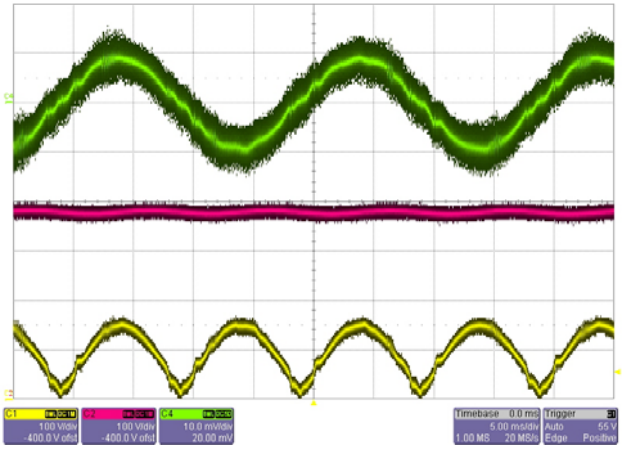

Figure 7. 110 Vac Input Voltage and Not Synchronized

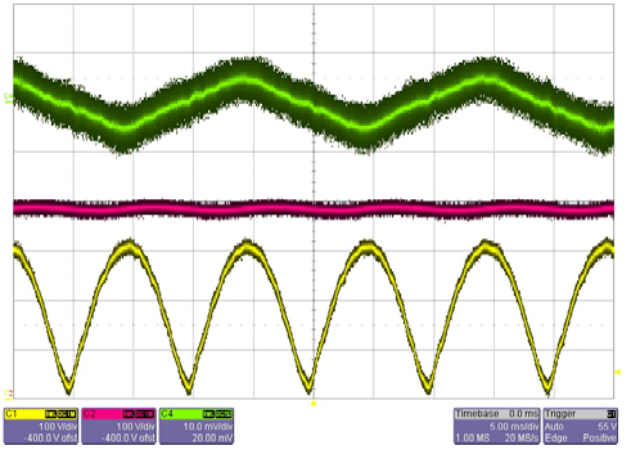

Figure 8. 220 Vac Input Voltage and Not Synchronized

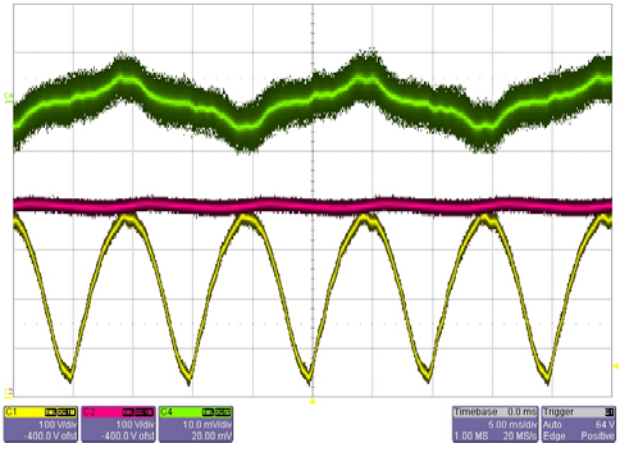

Figure 9. 260 Vac Input Voltage and Not Synchronized

Part III. Operating and Synchronized

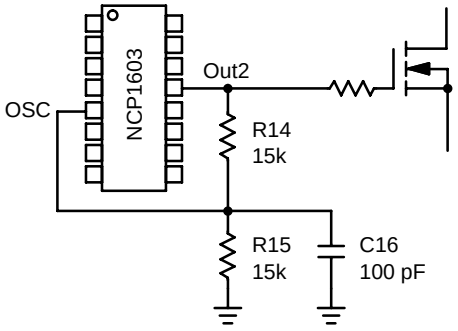

Figure 10. Synchronization Configuration

This part shows the circuit operating with the PFC and PWM sections are synchronized together. It is done by adding two 15 kΩ resistors (R14 and R21) as in Figure 10. The 100 pF capacitor here added as a decoupling filter for smoothing the synchronization signal to osc pin (Pin 5). The capacitor is essential because PFC performance can be degraded by noisy synchronization signal. The value of 100 pF is selected because too large value will result in big RC constant so that the osc pin voltage cannot reach 3.5 V and 5 V for synchronization. The result shows that the synchronization cannot offer a better efficiency in this circuit.

Input	Output	Efficiency	PF / THD
90 Vac 146.0 W	18.91 V 6.4 A	82.9%	0.998 / 4.5%
110 Vac 145.2 W	18.91 V 6.4 A	83.3%	0.997 / 5.3%
120 Vac 144.3 W	18.91 V 6.4 A	83.9%	0.996 / 6.6%
180 Vac 140.8 W	18.91 V 6.4 A	86.0%	0.993 / 5.8%
220 Vac 138.9 W	18.91 V 6.4 A	87.1%	0.982 / 11.4%
230 Vac 138.4 W	18.91 V 6.4 A	87.4%	0.976 / 15.3%
260 Vac 137.4 W	18.91 V 6.4 A	88.1%	0.939 / 31.3%

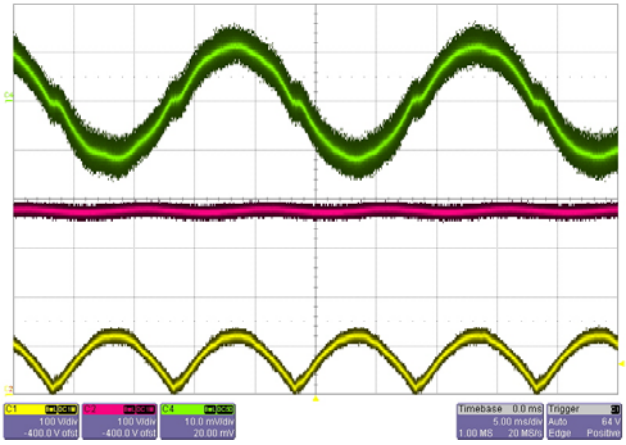

Figure 11. 90 Vac Input Voltage and Synchronized

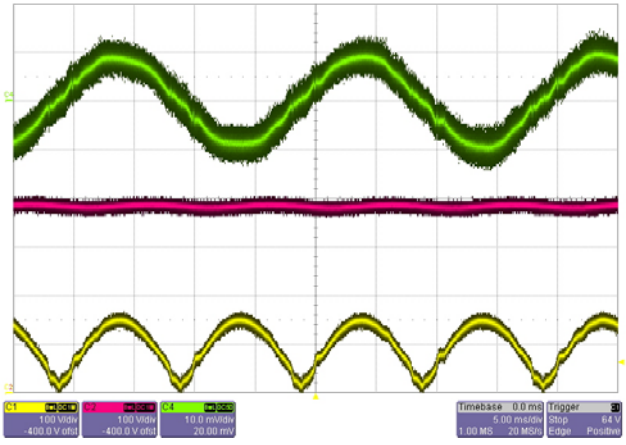

Figure 12. 110 Vac Input Voltage and Synchronized

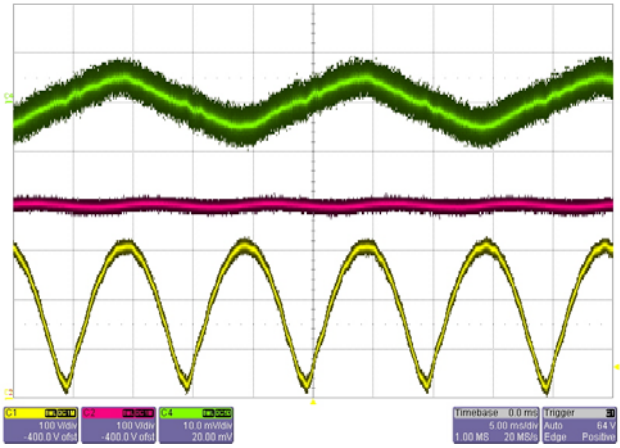

Figure 13. 220 Vac Input Voltage and Synchronized

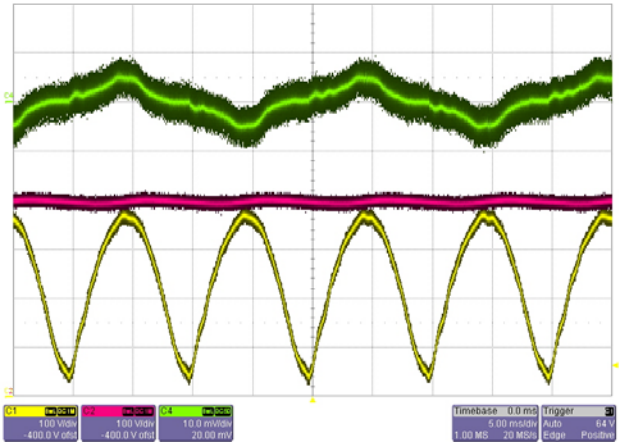

Figure 14. 260 Vac Input Voltage and Synchronized

Part IV. PFC On/Off Transition

PFC on/off toggling is an inherent feature of NCP1230 or NCP1603 circuit. The abrupt change of the PWM stage duty ratio may cause the PFC toggling on and off in boundary condition. In a PFC−on/off boundary condition, flyback circuit with higher input voltage needs lower duty ratio. Lower duty ratio means standby condition. It wants PFC−off. After PFC is off, the flyback input voltage goes lower and duty ratio goes higher. Higher duty ratio means normal operation condition. It wants the PFC−on. After PFC is on, the flyback input voltage goes higher again. Hence, the circuit may oscillate at the PFC−on/off boundary.

When resistor R22 is removed, the circuit goes toggling. In Figures 15 to 17, the upper trace is the output current with 1 A/div and the lower trace is the PFC output voltage with 100 V/div. In these figures, the input voltage is 110 Vac. The PFC stage is toggling when output current is 2.8 A in Figure 15. A resistor R22 (150 kΩ) is added between Vaux and CS2 pin. The PFC stage turns on when output is 3 A in Figure 16 and it turns off when output is 1.6 A in Figure 17.

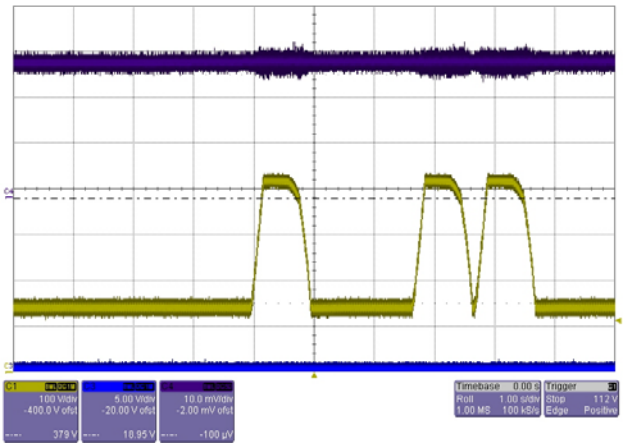

Figure 15. PFC Toggling in Boundary Condition when R22 Removed

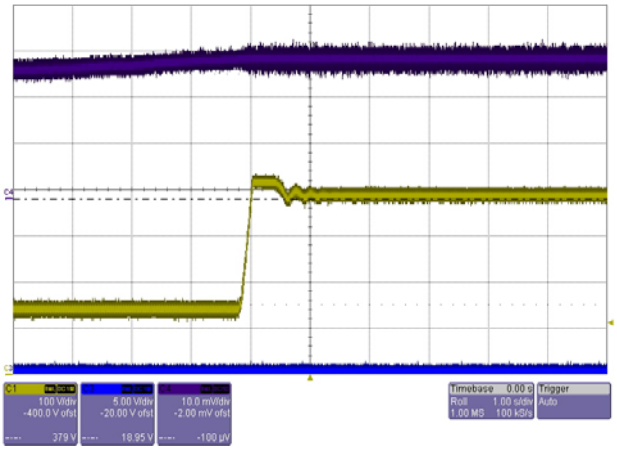

Figure 16. PFC Toggling Disappeared

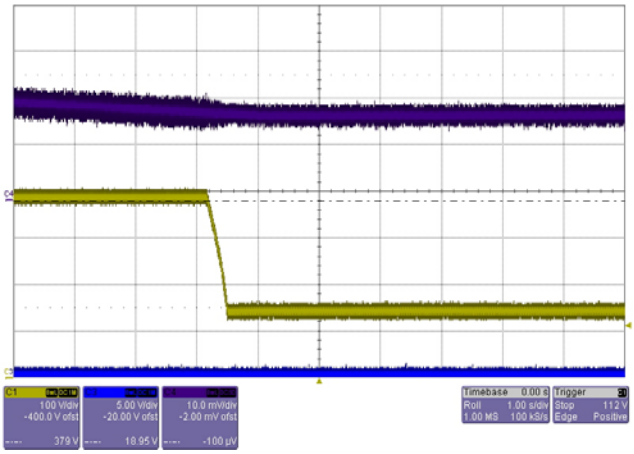

Figure 17. PFC Turns Off at Load Current

CONCLUSION

An example circuit using NCP1603 is presented. The design steps and measurement are covered. It is noted that the NCP1603 can perform a decent power factor correction, excellent standby performance and good efficiency at 120 W, 19 V, 6.4 A.

The PFC boost section is implemented in CRM and DCM. It needs very few external component for easier design and layout comparing to CCM−PFC. The DC−DC section is implemented in flyback that also needs the minimum external components. It makes the NCP1603 (or NCP1601 with NCP1230) application circuit is simple and minimal for low−power AC−DC application with PFC requirement.

Appendix I. Bill of Material of the NCP1603 19 V/6.4 A Example Circuit

Designator	Qty	Part No	Description	Manufacturer
F1	1	0465 02	250 V 2 A Delay Surface Mount Fuses	Littelfuse
L1	1	PCV−2−184−10	Inductor 10 A 180 μH	Coilcraft
L2	1	PCV−2−103−10	Inductor 10 A 10 μH	Coilcraft
T1	1	P3717−A	CM 25 mH, DM 1 mH filter, 3 A rms	Coilcraft
T2	1	SRW42EC−U16H014	Custom Transformer 420 μH, 5 A, 5.58:1:0.79	TDK
Q1	1	SPP11N60C3	11 A 600 V N−MOSFET	Infineon
Q2	1	SPP06N80C3	6 A 800 V N−MOSFET	Infineon
IC1	1	NCP1603D100	PFC/PWM Combo Controller	ON Semiconductor
IC2 − IC3	2	SFH615AA−X007	Optocoupler	Vishay
IC4	1	TL431AID	2.5 V 1% Voltage Reference, SO−8	ON Semiconductor
D1 − D4	4	1N5406	3 A 600 V Diode	ON Semiconductor
D5	1	MUR460	4 A 600 V Diode	ON Semiconductor
D6	1	MUR1100E	1 A 1000 V Diode	ON Semiconductor
D7	1	1.5KE250A	250 V TVS Zener Diode	ON Semiconductor
D8	1	MURS160	1 A 600 V Diode	ON Semiconductor
D9	1	MZP4745A	16 V @ 15.5 mA Zener Diode	ON Semiconductor
D10	1	MRA4005T3	1 A 600 V Diode	ON Semiconductor
D11 − D12	2	MBR16100CT	16 A 100 V Diode	ON Semiconductor
D13	1	1N5359B	24 V @ 1 mA Zener Diode	ON Semiconductor
D14	1	1N5923B	8.2 V @ 49.2 mA Zener Diode	ON Semiconductor
R1 − R2	2	WSL2512R0500FEA	0.05 Ω 1W SMD 1%	Vishay
R3 − R4	2	CCF55910KFKE36	910k Ω, axial 0.25W 1%	Vishay
R5	1	CRCW12066042F	60.4k Ω, SMD 1206 1%	Vishay
R6	1	CRCW120610R0F	10 Ω, SMD 1206 10%	Vishay
R7	1	CCF551K00FKE36	1k Ω, axial 0.25W 1%	Vishay
R8	1	N/A	bare wire, remove for disable PFC section	N/A
R9	1	CCF5510R0FKE36	10 Ω, axial 0.25W 1%	Vishay
R10	1	CRCW12063320F	332 Ω, SMD 1206	Vishay
R11 − R12	2	WSL2512R5000FEA	0.5 Ω 1W SMD 1%	Vishay
R13	1	HPS523−47k−5%	47k Ω, 4W axial 5%	Vishay
R14, R21	2	CRCW12061502F	15k Ω, SMD 1206	Vishay
R15	1	CRCW12064991F	4.99k Ω, SMD 1206	Vishay
R16	1	CRCW12061001F	1k Ω, SMD 1206	Vishay
R17	1	CRCW12061582F	15.8k Ω, SMD 1206	Vishay
R18	1	CRCW12062371F	2.37k Ω, SMD 1206	Vishay
R19	1	CCF55750RFKE36	750 Ω, axial 0.5W	Vishay
R20	1	CRCW120624R9F	25 Ω, SMD 1206	Vishay
R22	1	CRCW12061503F	150k Ω, SMD 1206	Vishay
R23	1	CRCW12064321F	4.32k Ω, SMD 1206	Vishay
R24	1	CRCW12061302F	13k Ω, SMD 1206	Vishay
C1	1	LE104	0.1 μF 275 Vac Film Capacitor	Okaya
C2	1	RE224	0.22 μF 275 Vac Film Capacitor	Okaya
C3	1	LE105	1 μF 275 Vac Film Capacitor	Okaya
C4 − C5	2	450AXW100M18X40	100 μF 450 V Aluminium Cap	Rubycon
C6	1	025YXG−470M00−10X16	470 μF 25 V Aluminium Cap 20%	Rubycon
C7	1	ERO610RJ4100M	1 nF 5 mm pitch Y2 cap	Evox Rifa
C8	1	630MMB473K	0.047 μF 630 V Film Capacitor 10%	Rubycon
C9 − C12	4	025YXG2200M12.5X30	2200 μF 25 V Aluminium Cap	Rubycon
C13	1	VJ1206Y222KXXA	2200 pF 25 V Ceramic Cap	Vishay
C14, C19 − C20	3	VJ1210Y824KXXA	0.82 μF 25 V Ceramic Cap	Vishay
C15, C17	2	VJ1206Y102KXXA	1 nF 25 V Ceramic Cap	Vishay
C16	1	VJ1206A101KXXA	100 pF 25 V Ceramic Cap	Vishay
C18	1	VJ1206A330KXXA	33 pF 25 V Ceramic Cap	Vishay
C21	1	VJ1210Y104KXXA	0.1 μF 25 V Ceramic Cap	Vishay
C22	1	VJ1206Y101KXBA	100 pF 100 V Ceramic Cap	Vishay
Heatsink	3	78065	Indian Chief 1.18” unfinished cut	Aavid
Heatsink Insulation	4	4672	TO−220 mica insultion	Keystone
AC Connector	1	770W−X2/10	IEC60320 C8 Connector	Qualtek
DC Connector	1	26−60−4030 or 009652038	3−terminal 3.96 mm distance male header	Molex

Appendix II. The PCB Layout

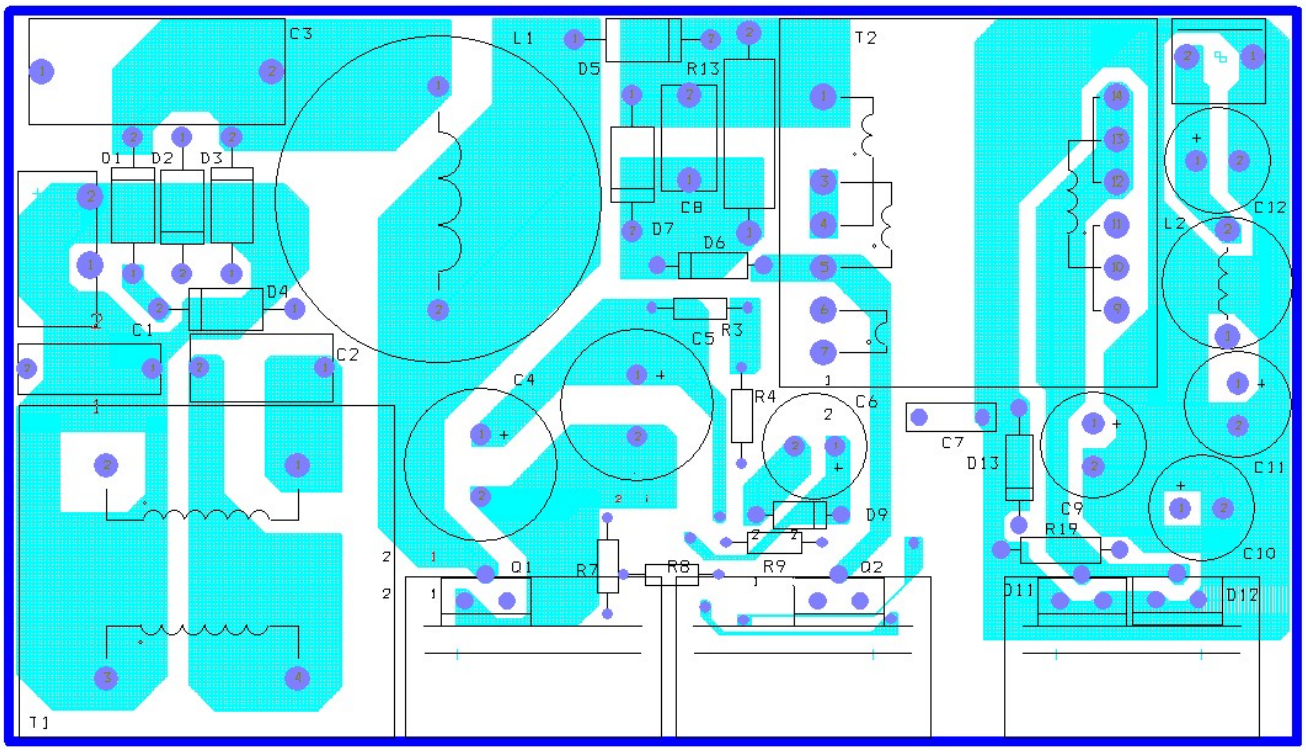

Figure 18. Top Layer Layout

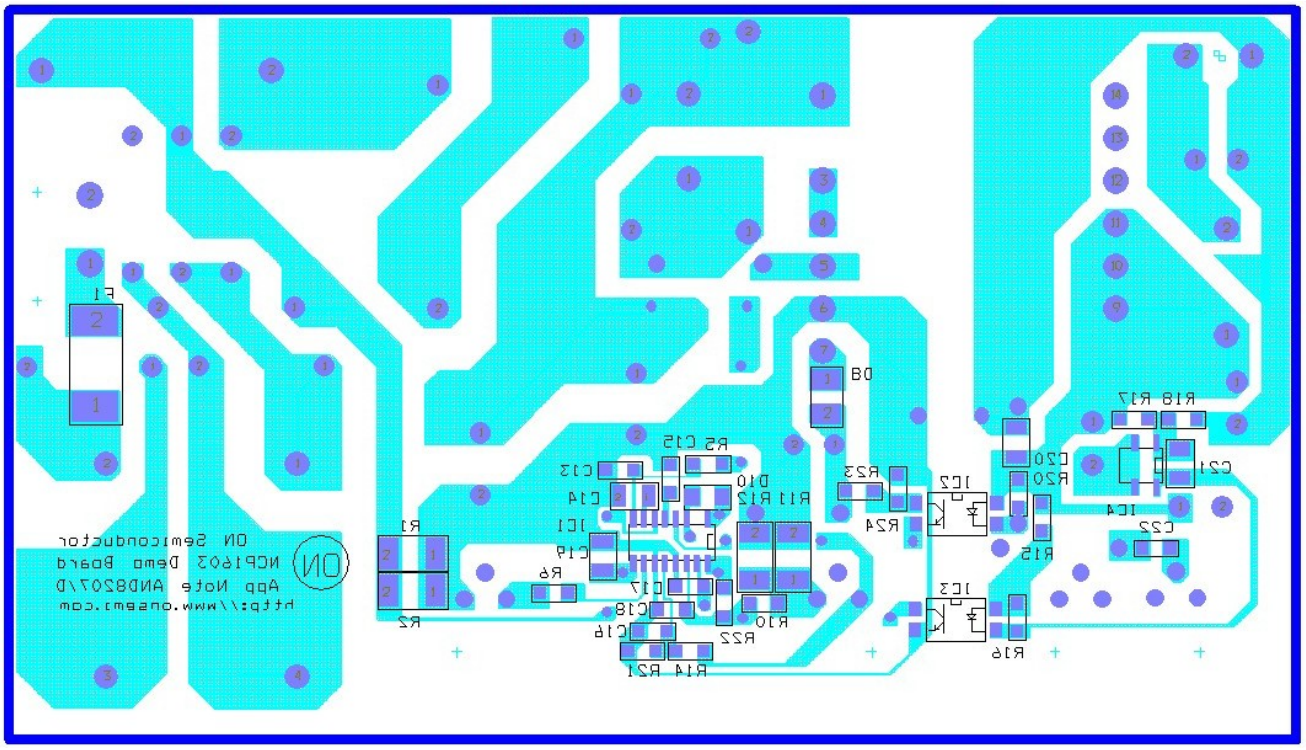

Figure 19. Bottom Layer Layout

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